REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of January 24, 2008 (hereinafter "Office Action"). Applicants especially appreciate the indication that Claims 2 - 7, 9 - 13, 20 - 22, and 24 recite patentable subject matter. Rather than writing any of the allowable claims in independent form at this time, Applicants respectfully submit that the cited reference does not disclose or suggest all of the recitations of the independent claims. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Section 112 Rejection

Claims 14 - 18 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. (Office Action, page 2). With regard to independent Claim 14, the Office Action alleges that the preamble, "[a] method for distributing a clock signal," renders the claim as a whole unclear because there is no distribution step recited. (Office Action, page 2). In response, Applicants have amended the preamble of Claim 14 to recite "[a] method of generating clock signals." With regard to both Claims 14 and 15, the Office Action alleges that the recitations directed to the error signals are unclear. (Office Action, page 2). While Applicants do not agree that the recitations directed to the error signals in Claims 14 and 15 render these claims unclear, to advance prosecution and to facilitate an early allowance of the present application, Applicants have amended Claims 14 and 15 as set forth above to change the order of the recitations in these claims so that the error signals are recited before the clock signals are recited. In view of these amendments and supporting remarks, Applicants respectfully submit that Claims 14 - 18 satisfy the requirements of 35 U.S.C. §112.

Independent Claims 1, 8, 14, 19 are Patentable

Independent Claims 1, 8, 14, and 19 stand rejected under 35 U.S.C. §103(a) as being

unpatentable over U. S. Patent No. 5,638,410 to Kuddes (hereinafter "Kuddes"). (Office Action, page 3).

Independent Claim 1 is directed to a clock distribution circuit and includes the following recitations:

> a first clock circuit that is configured to generate a first clock signal responsive to an error signal;
> a second clock circuit that is configured to generate a second clock signal responsive to the error signal; and
> a phase detector circuit that connects the first clock circuit to the second clock circuit and is configured to generate the error signal responsive to the first and the second clock signals.

Independent Claims 8, 14, and 19 include similar recitations. According to the recitations of Claim 1, first and second clock circuits generate respective clock signals responsive to the same error signal, which is generated by a phase detector circuit that connects the first and second clock circuits.

In rejecting Claims 1, 8,14, and 19, the Office Action cites the phase locked loop circuit 102, the phase locked loop circuit 122, the clock signal $\phi 1$, and the clock signal $\phi 2$ shown in FIG. 1 of Kuddes as corresponding to the first clock circuit, second clock circuit, first clock signal, and second clock signal recited in independent Claim1, respectively. (Office Action, page 3). The Office Action further cites the phase detectors 104 and 124 shown in FIG. 1 of Kuddes as corresponding to the phase detector circuit recited in independent Claim 1. (Office Action, page 3). In sharp contrast to the recitations of Claim 1, however, the phase locked loop circuits 102 and 122 do not generate their respective clock signals responsive to an error signal generated by one of the phase detector circuits 104 and 124. Rather, the output signals from the phase detector circuits 104 and 124 are processed and used to adjust the delay applied through the digital delay lines 112 and 132, respectively.

The Office Action acknowledges that Kuddes fails to disclose generating the first and second clock signals responsive to an error signal as recited in independent Claim 1, but alleges it would be obvious to modify Kuddes so that the phase locked loop circuits 102 and 122 generate their output signals responsive to an error signal generated by one of the phase

detector circuits 104 and 124. (Office Action, page 3). The reasoning for this modification is stated as follows:

> Therefore, it would have been obvious to a person of ordinary skill in the testing art, at the time the invention was made, to feed back the error signal to the first and second clock circuits so that based on that error signal the first and second clock signals are generated, these clock signals are then applied to the phase detector to generate error signal responsive to phase different between the first and second clock signals so that the error signal can be corrected by adjusting phase error to synchronize phases of the clock signals. (Office Action, page 4).

It appears that the reasoning alleged for modifying Kuddes is derived from hindsight reasoning in which Applicants' claim language is used as a roadmap. Kuddes provides no suggestion for modifying the phase locked loop circuits 102 and 122 to generate their clock signals responsive to error signals generated by one or both of the phase detector circuits 104 and 124. As explained above, the error signals output from the phase detector circuits are processed and used as delay control signals to drive the digital delay lines 112 and 132, respectively. Kuddes provides no suggestion of why it would be desirable for the phase locked loop circuits 102 and 122 to use delay control signals to generate their respective output clock signals. Kuddes actually states that "[t]he specific structures of PLL 102 and 122, and the techniques used to generate the clock signals $\phi 1$ and $\phi 2$ are not needed to understand the concept of the invention." (Kuddes, col. 3, lines 23 - 26). Thus, Kuddes is silent with respect to possible modifications to the phase locked loop circuits 102 and 122 as the particulars of their structures and operations are deemed irrelevant to Kuddes' clock circuitry.

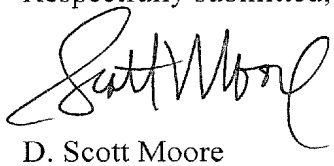
Applicants submit, therefore, that independent Claim 1 is patentable as Kuddes fails to disclose or suggest first and second clock circuits that generate respective clock signals responsive to the same error signal, which is generated by a phase detector circuit that connects the first and second clock circuits. Independent Claims 8, 14, and 19 include similar recitations and are patentable over Kuddes for at least the same reasons.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 1, 8, 14, and 19 are patentable over Kuddes and that Claims 2 - 7, 9 - 14, 15 - 18, and 20 - 24 are patentable at least per the patentability of independent Claims 1, 8, 14, and 19.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



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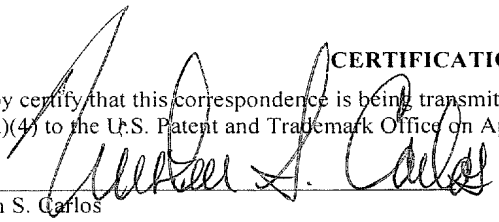

Kirsten S. Carlos